Lithography Strategy for 65nm Node

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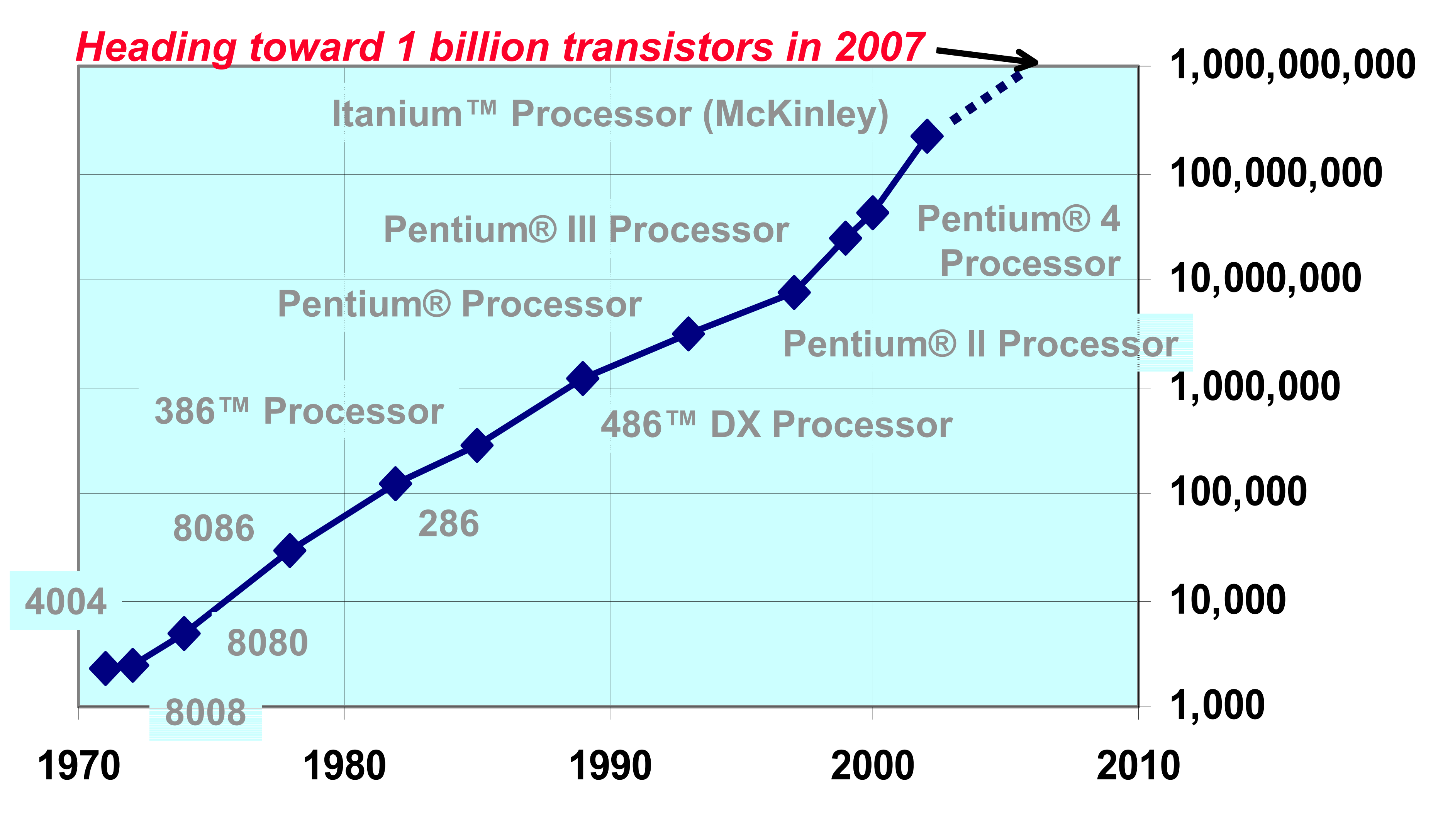
Lithography Strategy for 65nm Node

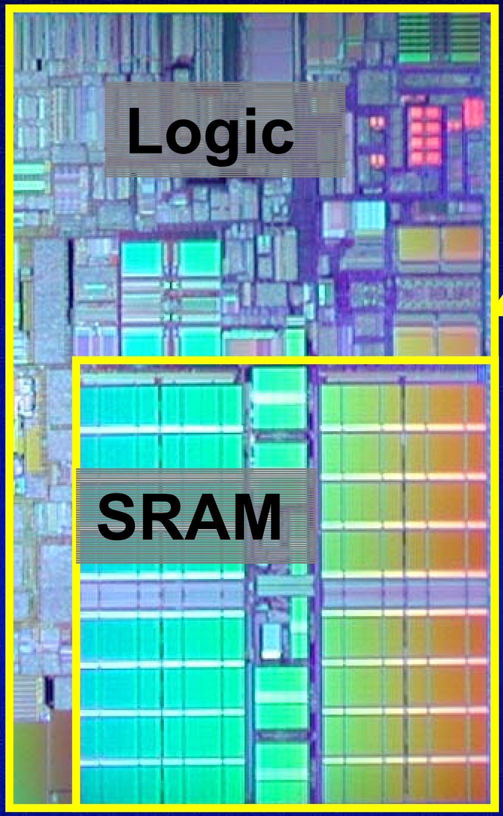
Outline

1. Scaling Trends
2. Parallel Approach:
   - A. 157nm Lithography
   - B. 193nm Lithography
- Mask Making challenges
- Conclusion

Moore's Law Continues



Same process for Logic and SRAM

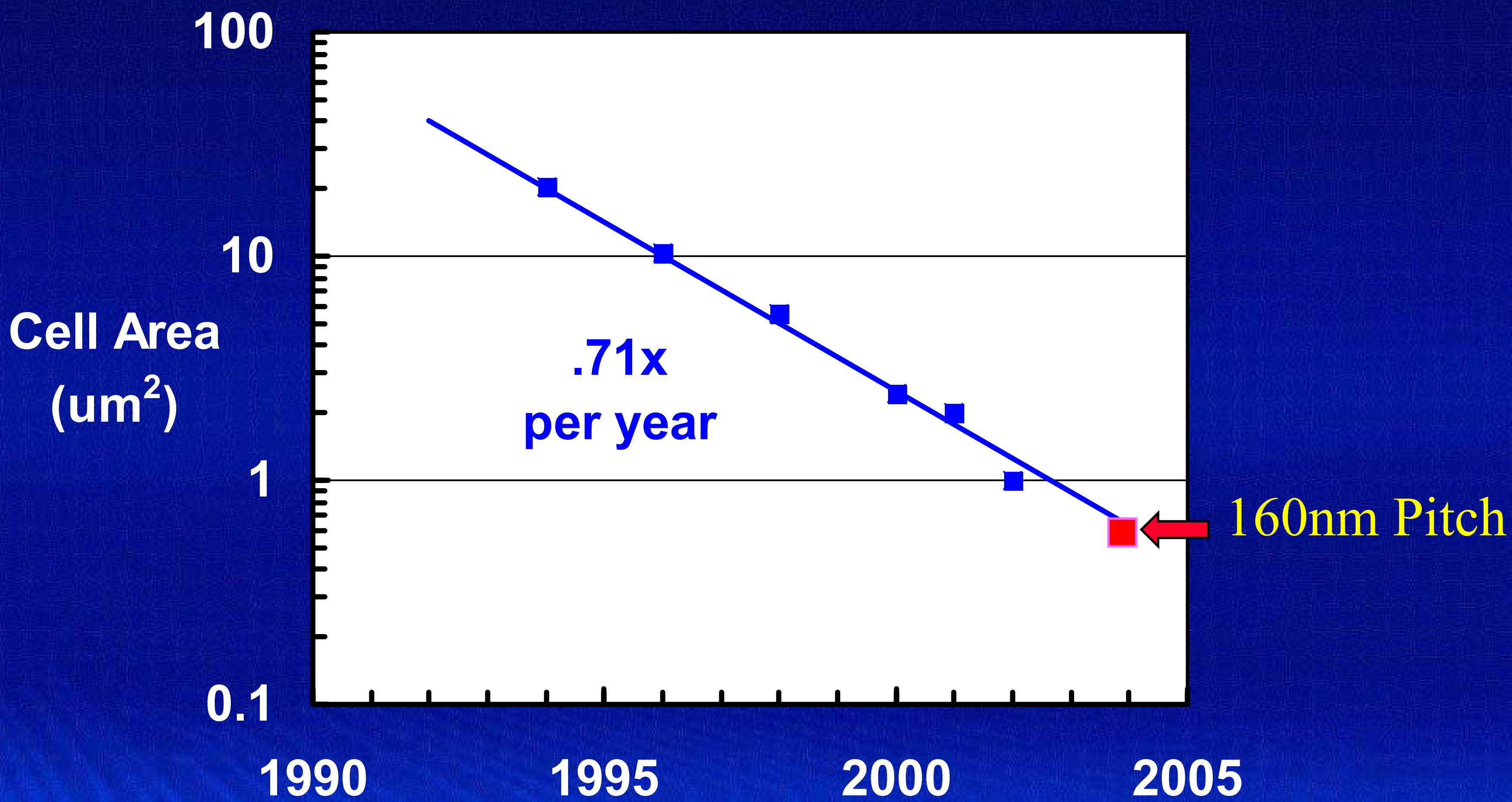


0.13 μm
Pentium® III CPU

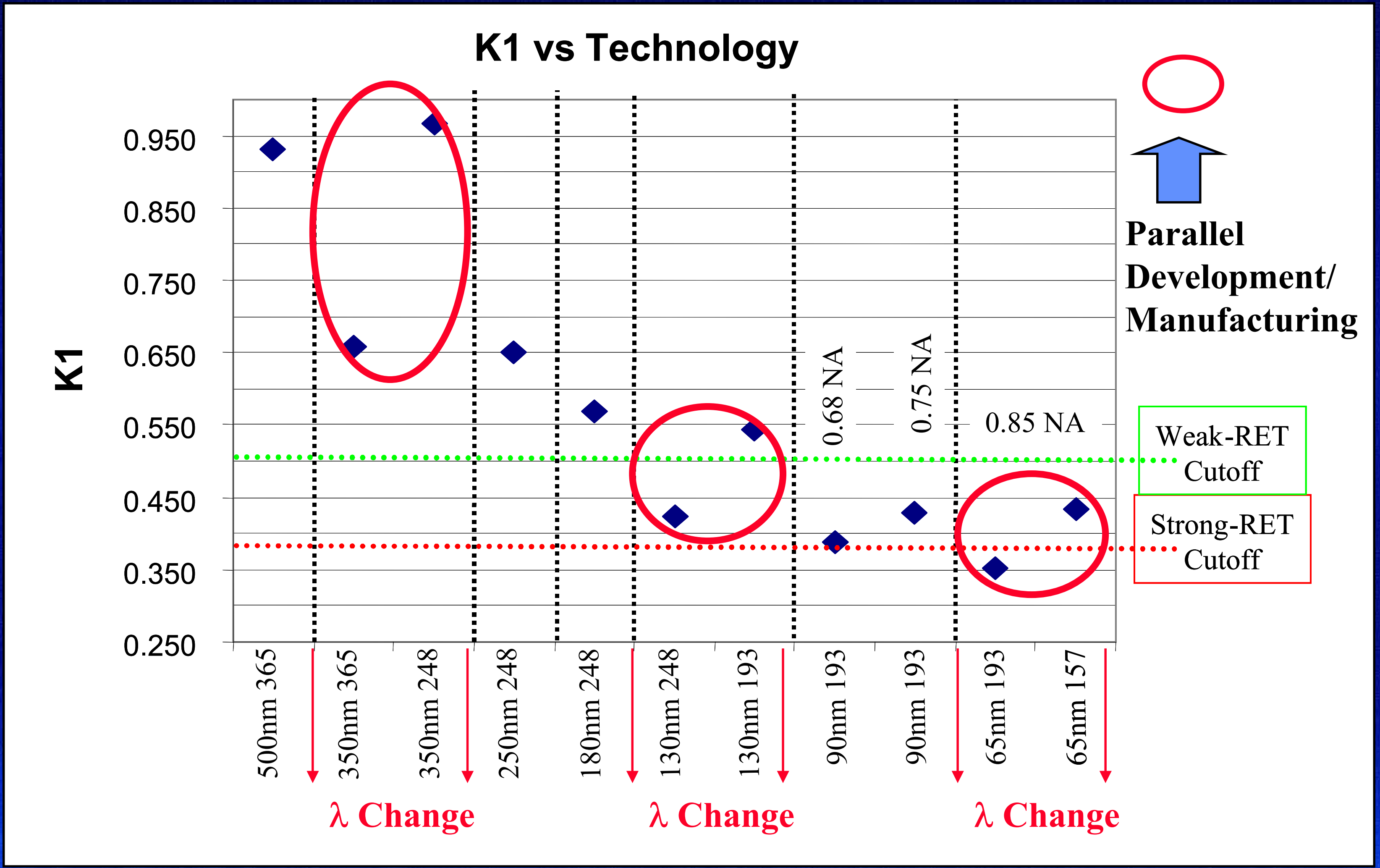
1 μm^2 SRAM cell
(six transistors)

- Modern microprocessors use the same transistors and interconnects for both logic and SRAM circuit blocks
- The process used to make 90 nm SRAM chips is the same process for 90 nm microprocessors

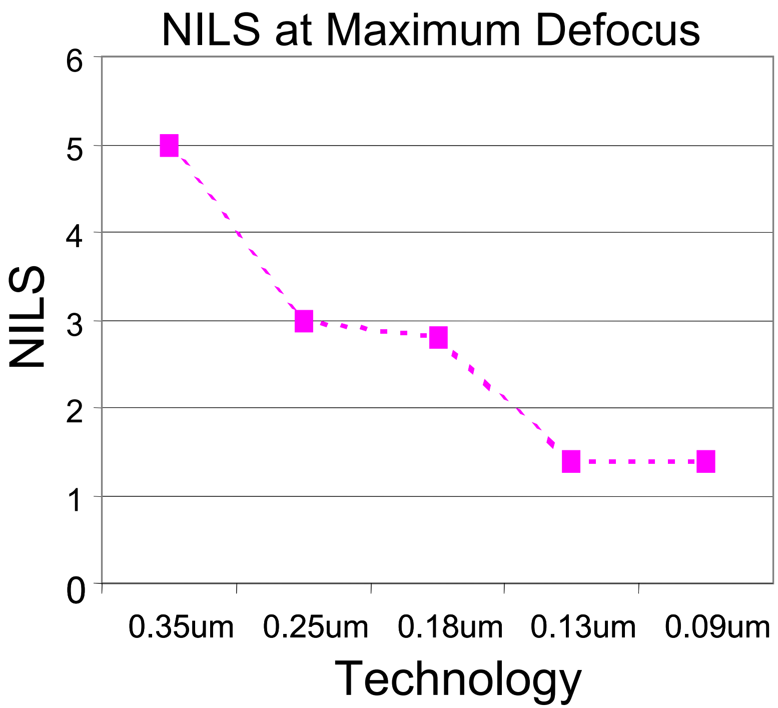
Intel SRAM Cell Size Trend



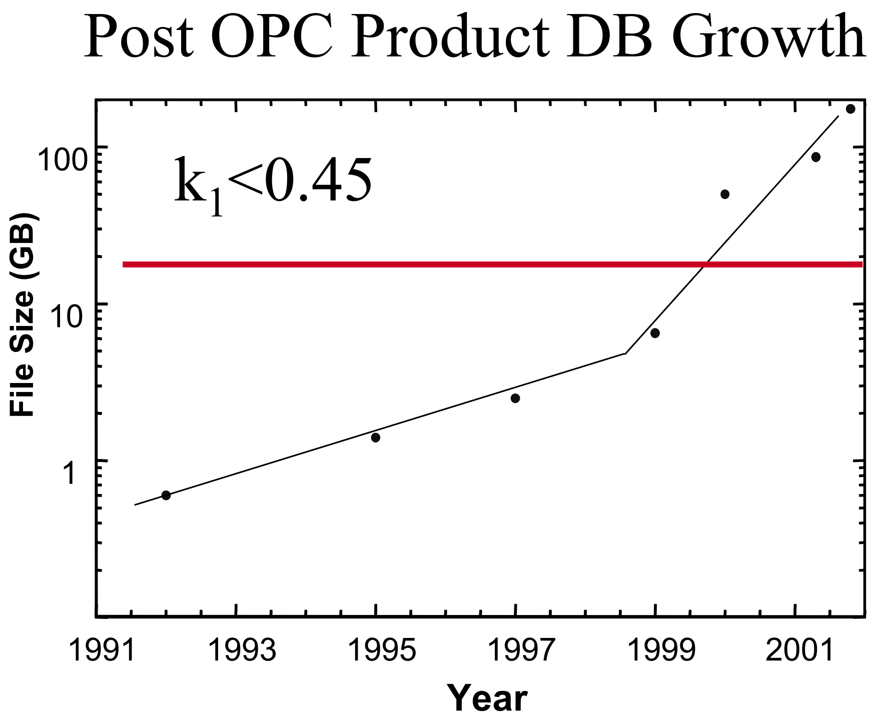
Lithography Complexity Trend and Management: Dual Path at Wavelength Change



Resist and OPC Advances

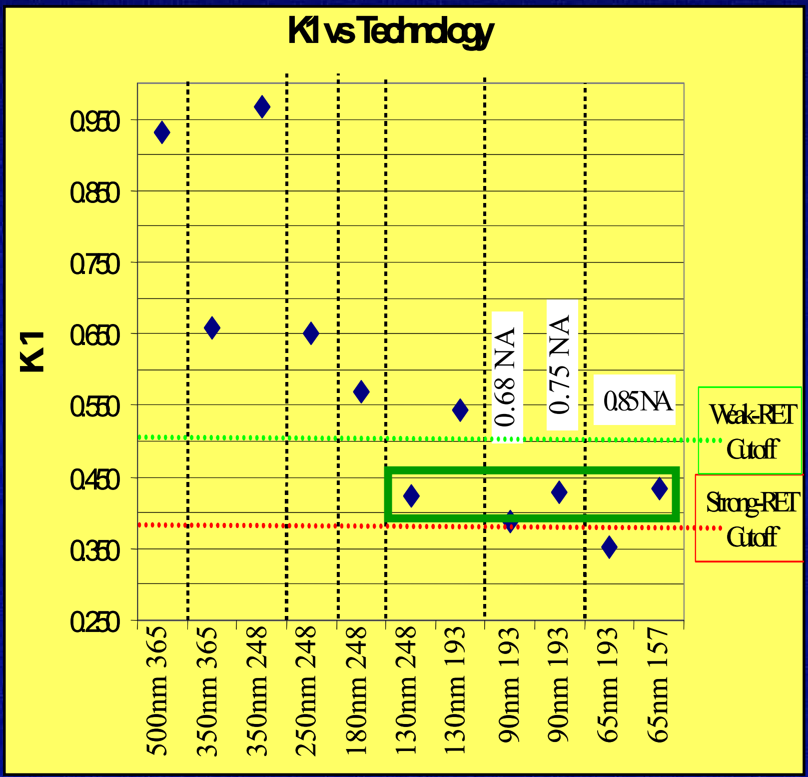


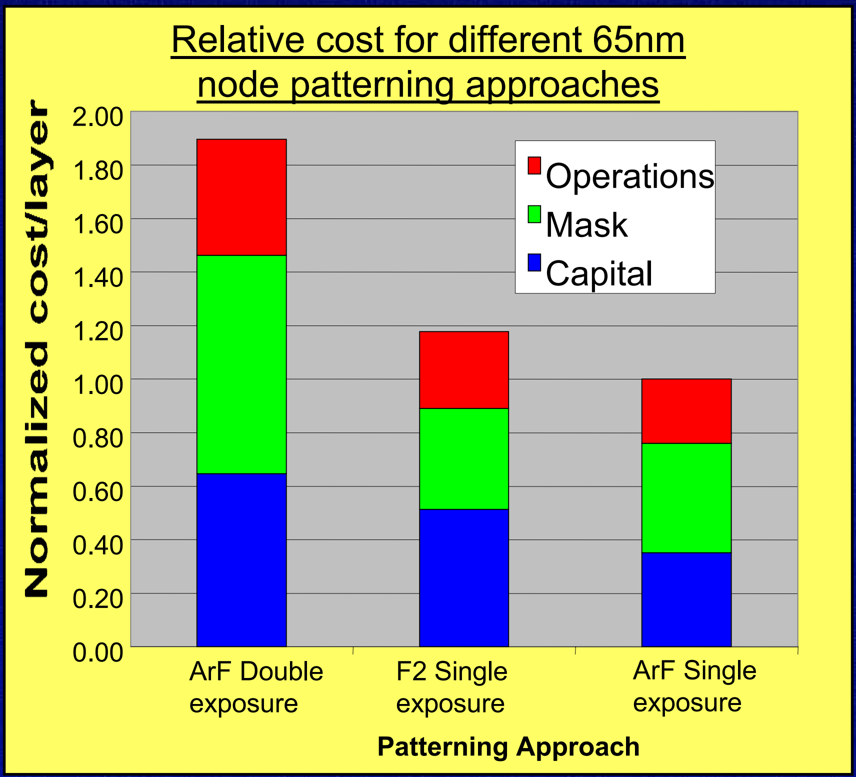
Improvements in Resist Enabled Patterning at lower image contrast



Growth in OPC use and complexity enabled lower k_1 patterning while increasing database sizes

65nm Node –157nm Lithography





Proven "Weak" RET Solutions **Lower Cost**

65nm Node –157nm Lithography

Major Advances:

- ✓ CaF_2 Lens design issues Resolved
- ✓ CaF_2 Investments Significant, Yields to 157nm Specs Improving
- ✓ 1st Commercial Resist Available
- ✓ COG and EPSM blanks Available
- ✓ "Soft" Pellicle transmission > 98%
- ✓ F_2 Lasers Available
- ✓ All major exposure tools suppliers plan for Shipments of 0.85NA Production Tools in 2004 - 2005

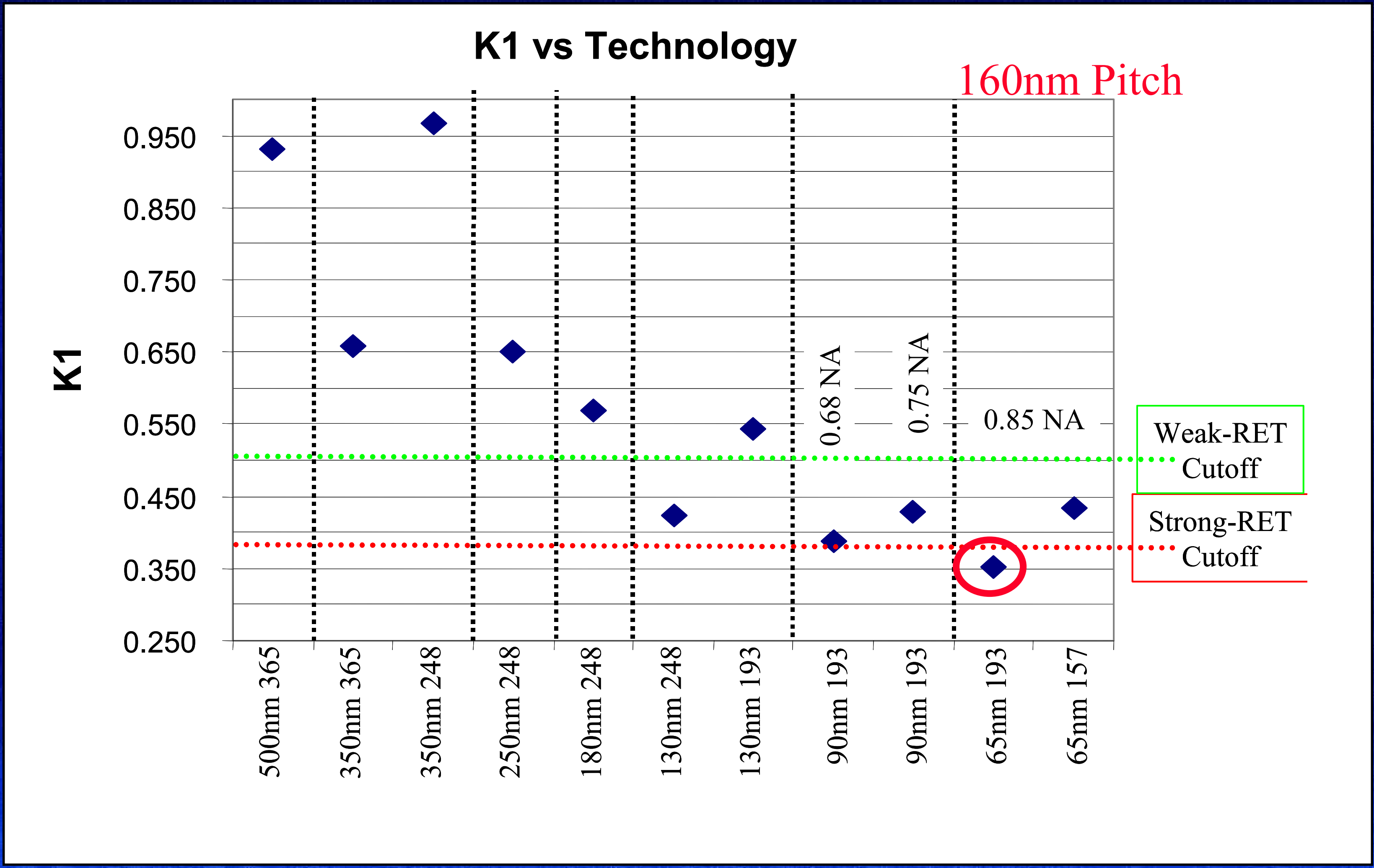
65nm Node
157nm Lithography Challenges

Exposure Tool Introduction Timing

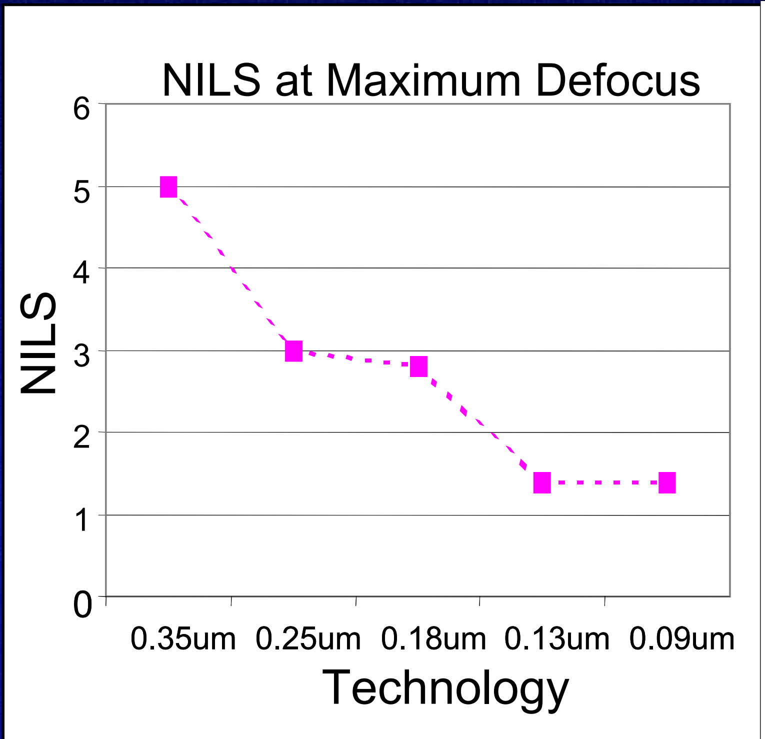
- No Process Development Exposure Tools until Q3’03
- No Production Exposure Tools until H2 2004
- 157nm can capture significant part of 65nm manufacturing if no further slips of tool delivery
- Intel will utilize 157nm tools as soon as they are ready for volume manufacturing

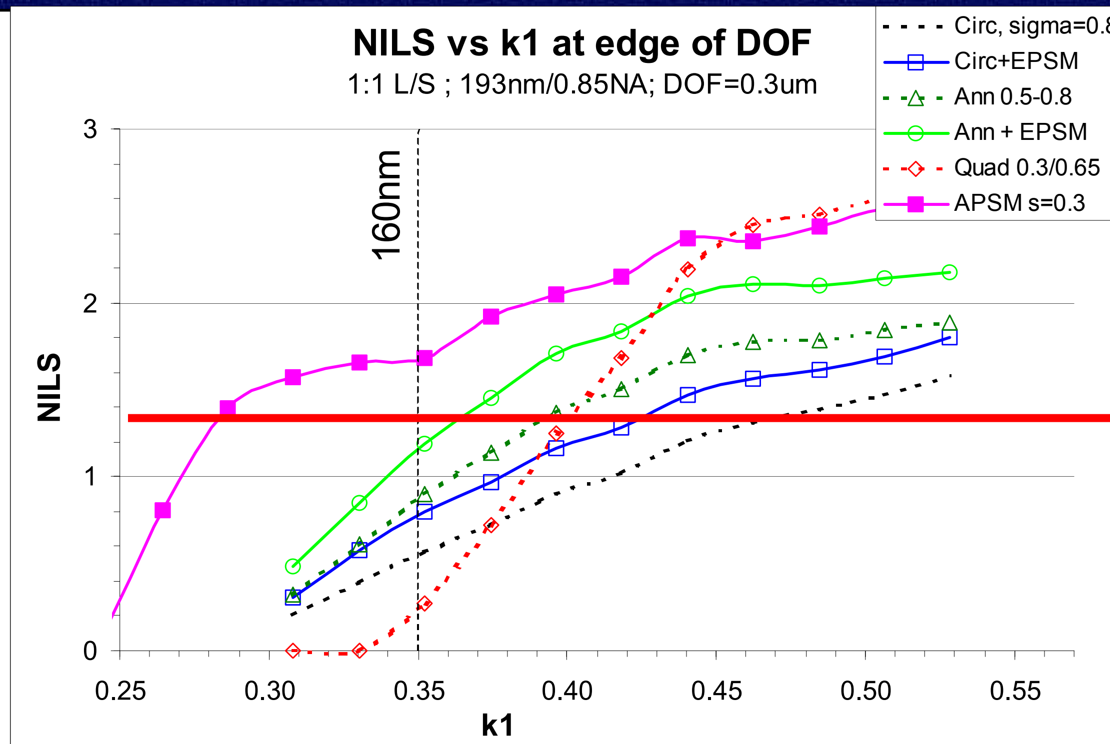
Particle Protection issue must be resolved

65nm Node –193nm Lithography



65nm Node –193nm Lithography

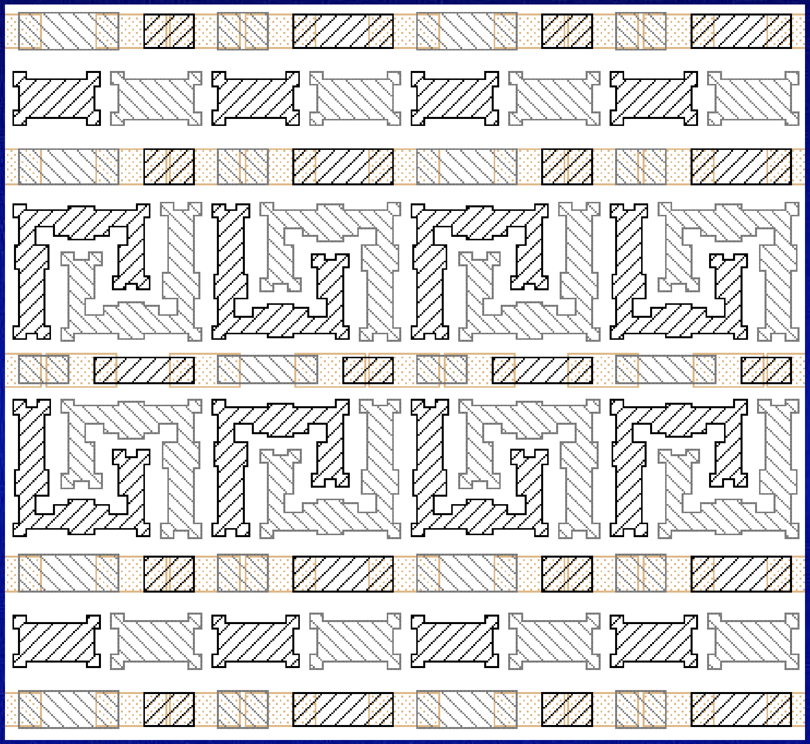


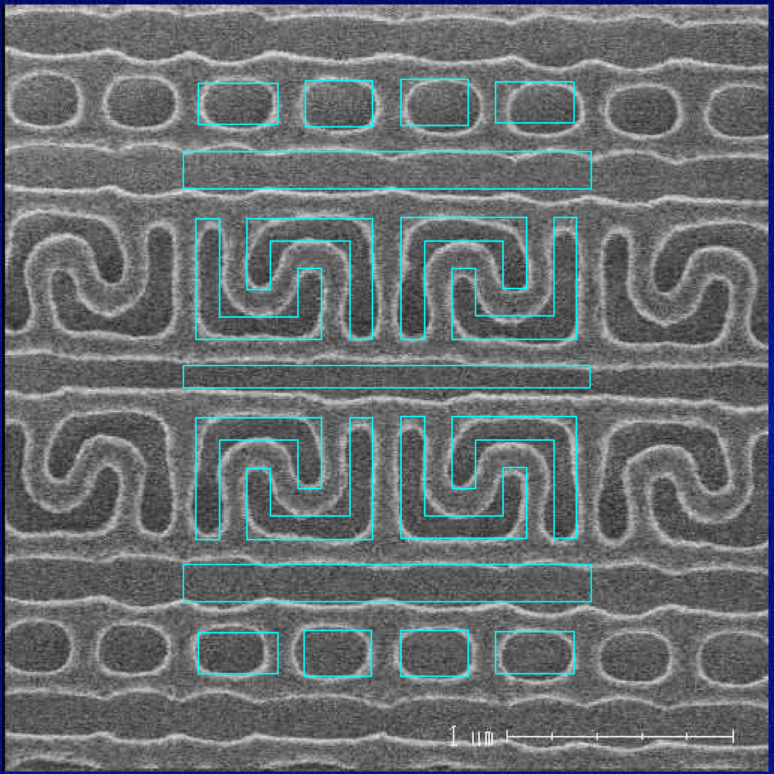


Analysis of options available with 193nm resists equal in performance to advanced DUV resists leads to the conclusion that strong RET will be required to support patterning 160nm pitches with 0.85NA 193nm

65nm Node –193nm Lithography

Critical Metal Layer DF AltPSM Patterning (SRAM)





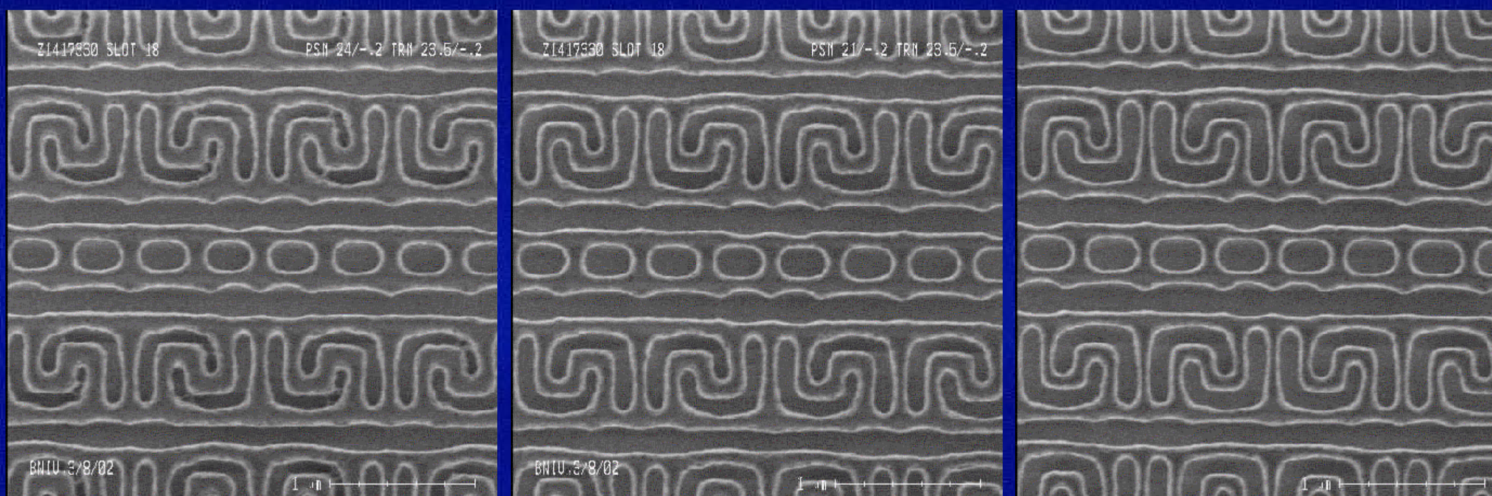
SRAM Phase assignment, Simple, rule based OPC

SRAM 193nm Patterning at $k_1 = 0.35$

65nm Node –193nm Lithography

Metal AltPSM Dose Latitude at k_1=0.35 >10%

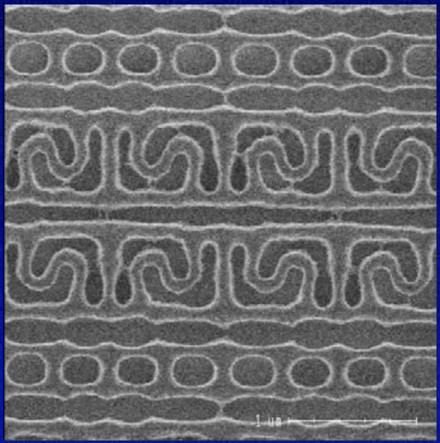
Enom – 13% Enom Enom + 13%



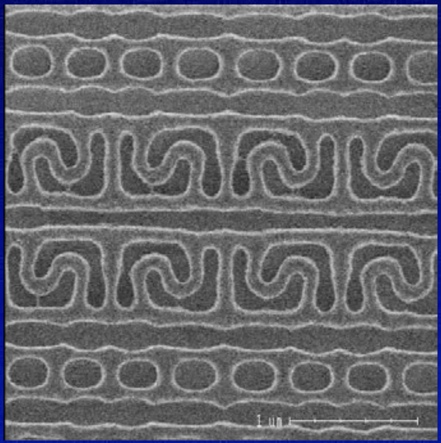
AltPSM is very effective to protect from bridging

65nm Node –193nm Lithography

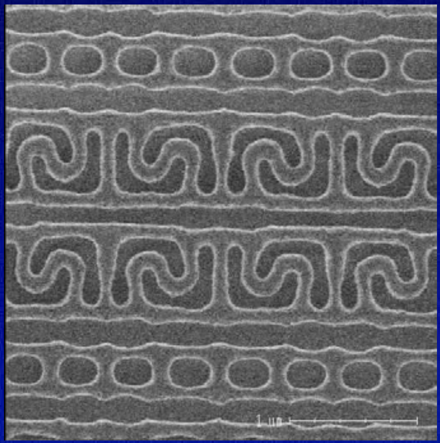
Metal AltPSM Depth of Focus at k_1=0.35 >0.40 um



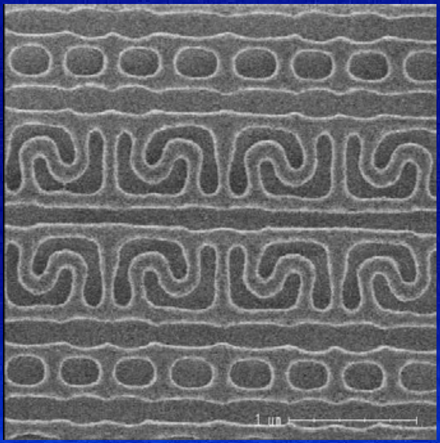
-0.25um/-0.38um



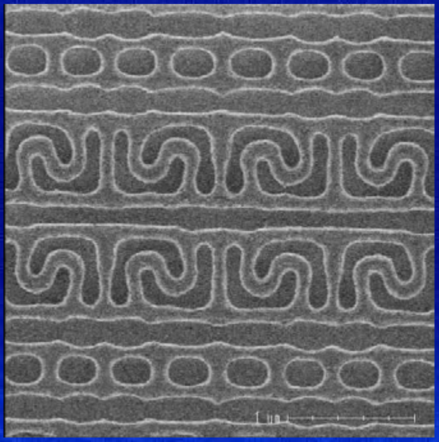
-0.15um/-0.28um



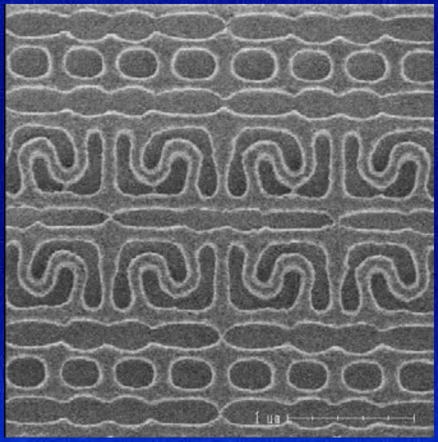
-0.05um/-0.18um



0.05um/-0.08um



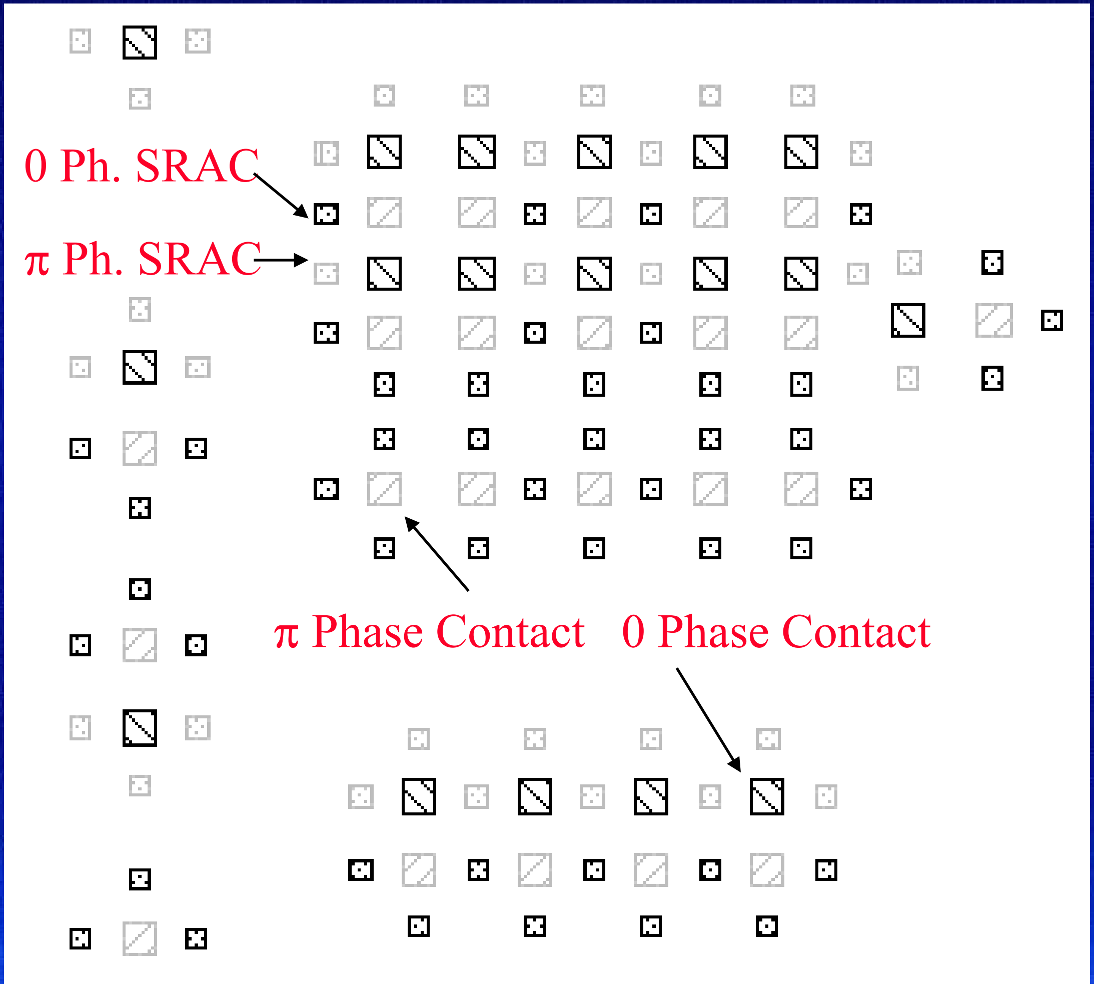
0.15um/0.02um



0.25um/0.12um

65nm Node –193nm Lithography

Contact Layer - Single Exposure AltPSM



Phase Assignment for Random Logic Contact with Single Exposure Sub-Resolution Phase Assisted contacts.

Manufacturable:
Bridge resistant,
MEEF = 4-5 Allows
SRAC=0.85CON

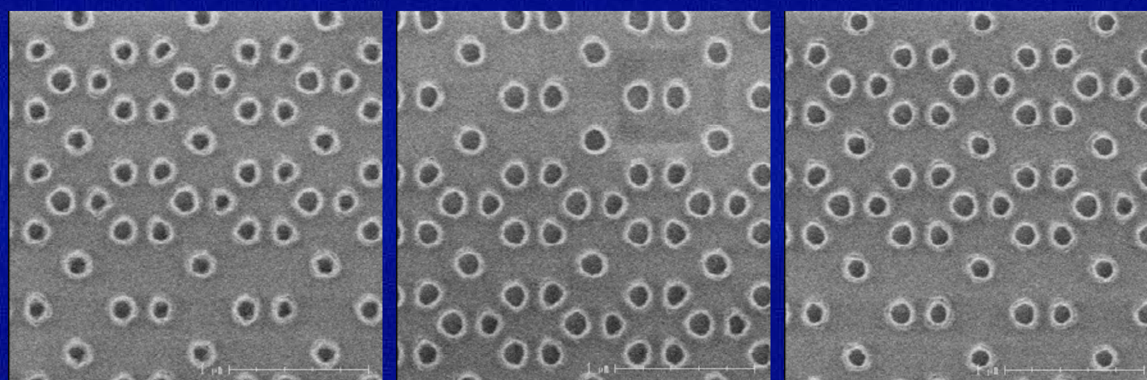
Intel

65nm Node –193nm Lithography

Contact Layer - Single Exposure AltPSM

Depth of Focus at k_1=0.35 > 0.4 μm

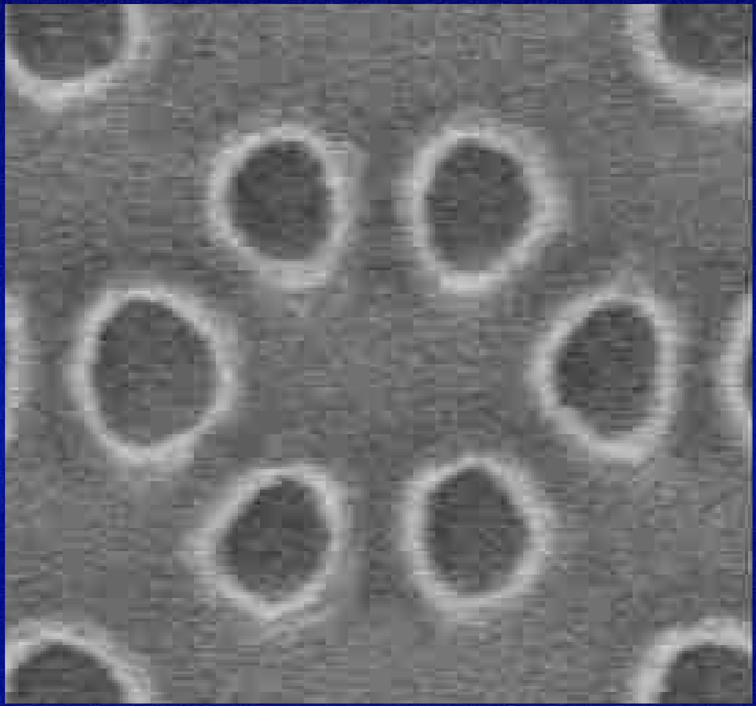
Fnom –0.2um　　Fnom　　Fnom +0.2um



SRAM Contact printed with AltPSM +SRAC

65nm Node –193nm Lithography

Contact Layer - Single Exposure AltPSM Limitations



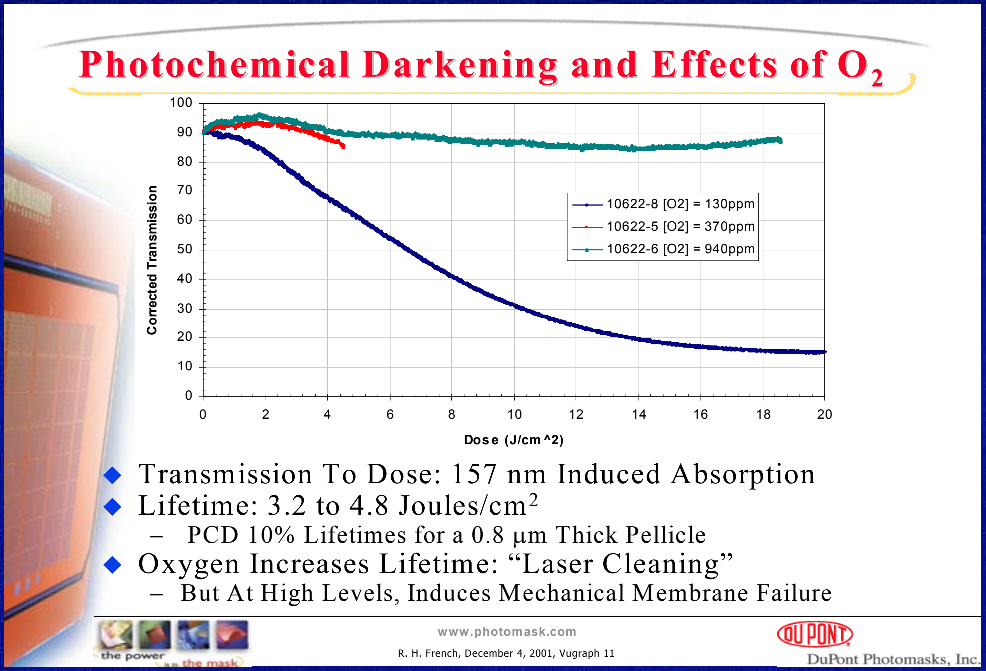
Destructive Interference
Results in non-circular CON

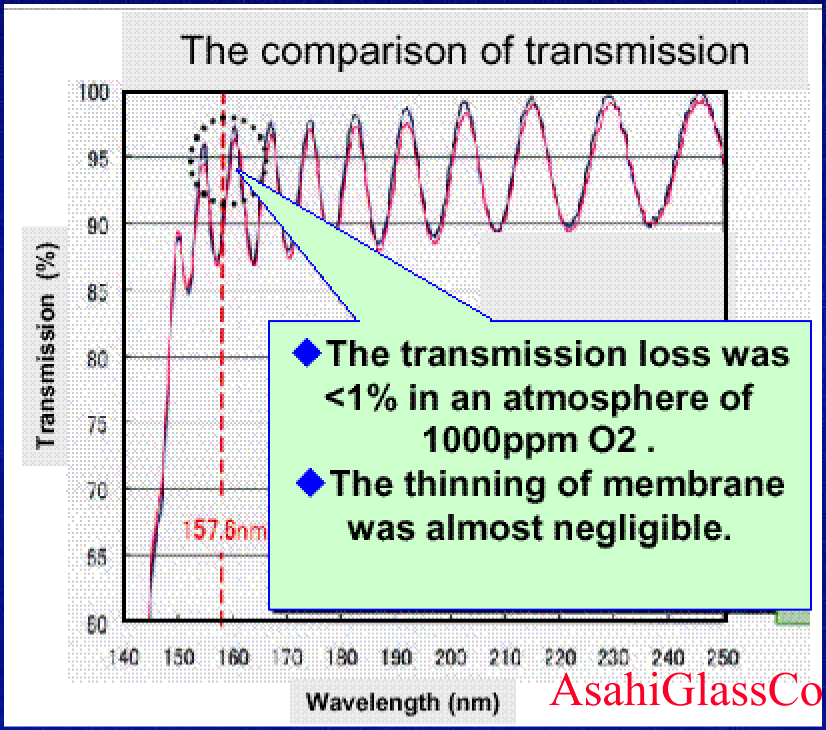
65nm Node Lithography
Mask Making Challenges – 157nm

- No need for AltPSM to pattern pitches at k_1=0.43
- Major Focus –Mask Dimensional Control
  - EPSM Blanks
- Critical need –Particle Protection Solution:
  - Hard Pellicle – not proven
  - Replaceable pellicle – possible but inconsistent with 2005 HVM
  - Polymer Pellicle most desirable

65nm Node Lithography
Mask Making Challenges – 157nm

Excellent progress on Polymer Pellicle Transmission





Polymer pellicle needs 400x durability improvement – <u>Mechanism of Photochemical Darkening must be understood and negated.</u>

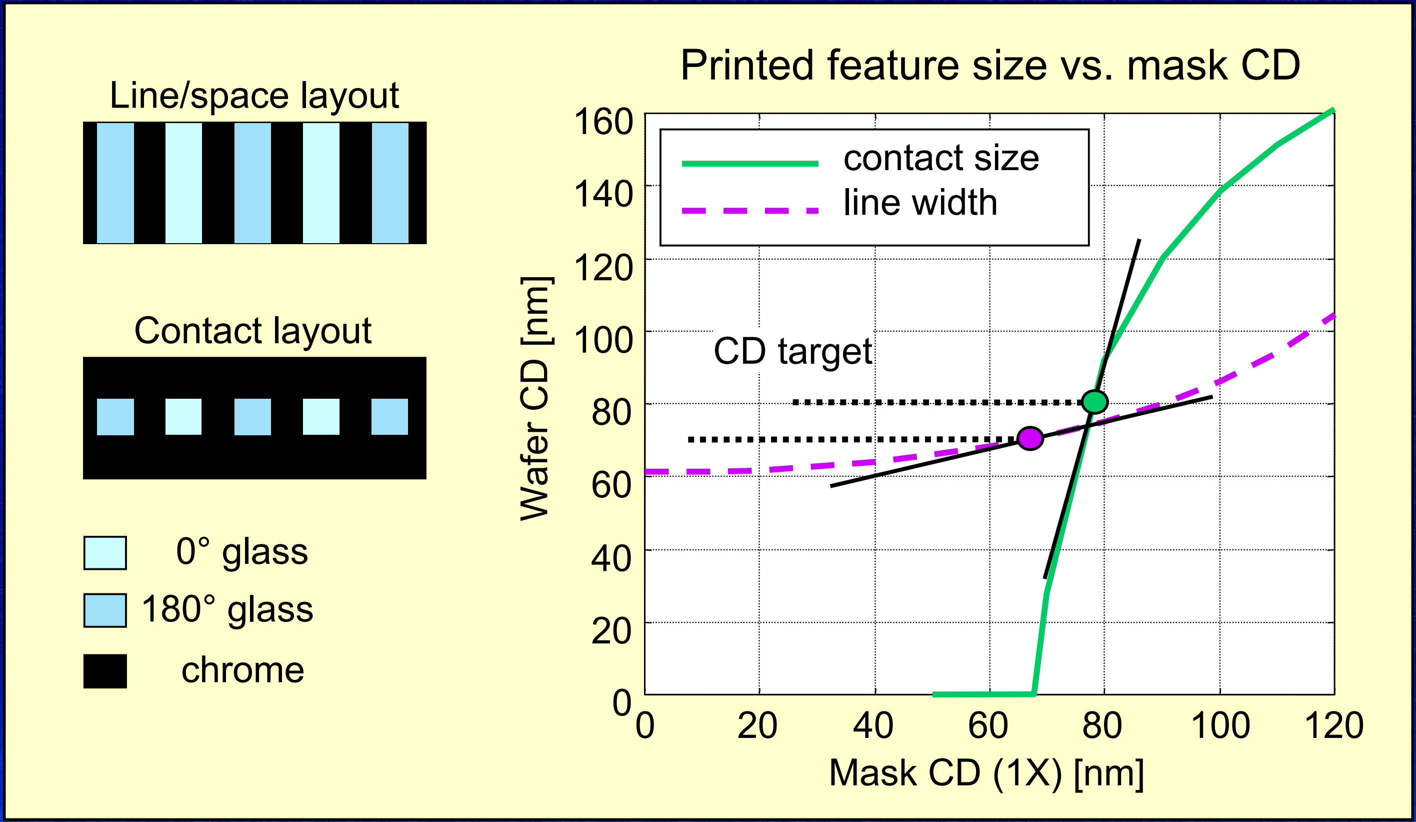
65nm Node Lithography
Mask Making Challenges – 193nm

- Strong RET (AltPSM) needed to pattern pitches at K1=0.35

- Major AltPSM Masks *specific* issues:
- Phase Control
- Image Imbalance Control
- Inspection
- Phase Repairs

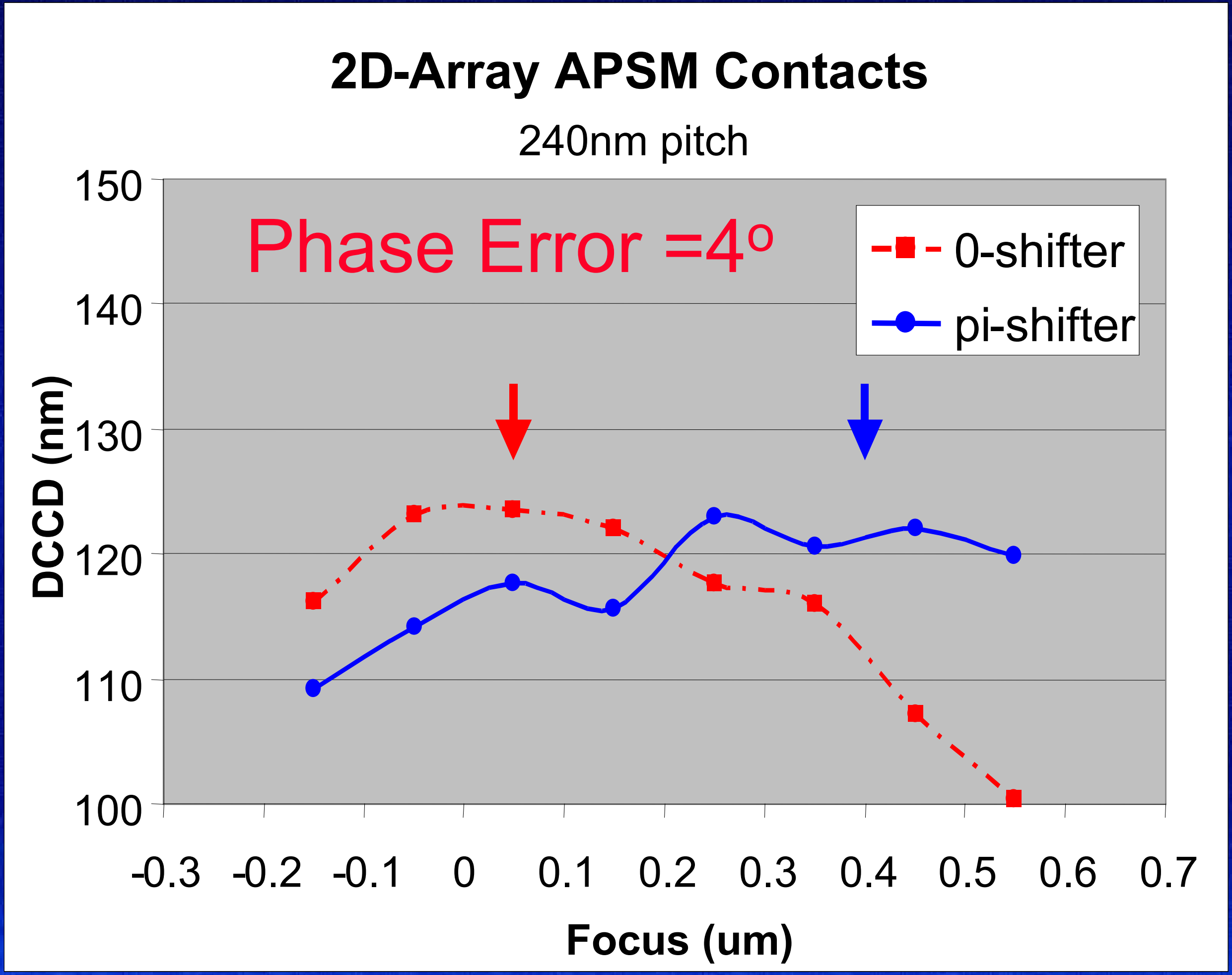
65nm Node Lithography
Mask Making Challenges – 193nm

- **AltPSM MEF sensitivity = OPC Complexity**



Mask Making Challenges – 193nm

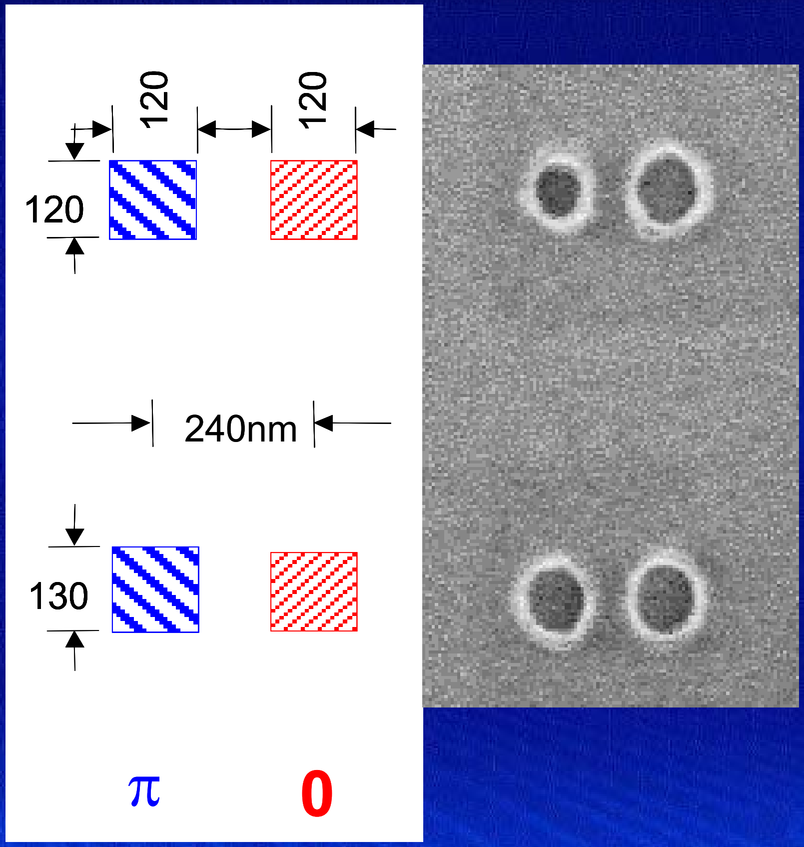
AltPSM Phase Control = Process Control



Max Phase Error <2º needed

65nm Node Lithography
Mask Making Challenges – 193nm

AltPSM Intensity Imbalance = Process Control



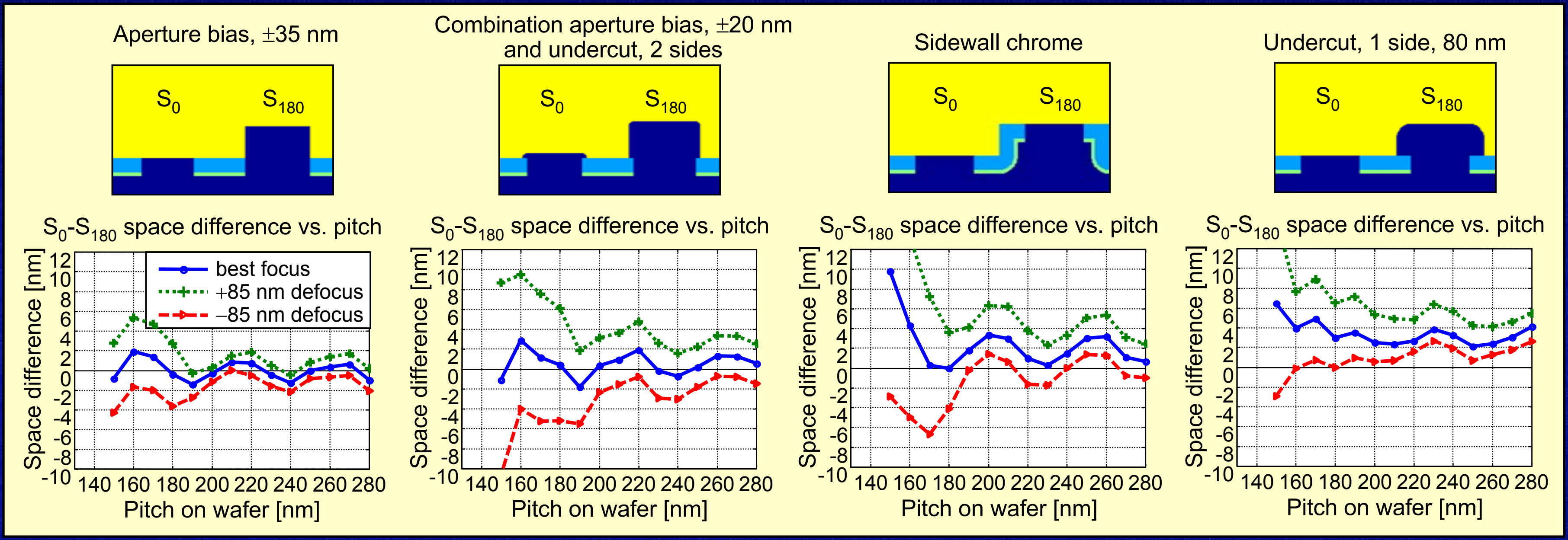
Contact Layer at k1=0.35
Single Exposure AltPSM

Uncorrected Intensity balance
Results in severe CD issues

0/π Intensity imbalance can be corrected by π contact Sizing.

65nm Node Lithography
Mask Making Challenges – 193nm

AltPSM Intensity Imbalance = Process Control



Aperture bias | Aperture bias+Cr Undercut | SCAAM | One Side Cr Undercut

Intensity imbalance for line/space modeled for 0.85NA, 193nm
Cr = 280nm on the mask, Pitch and Defocus varies

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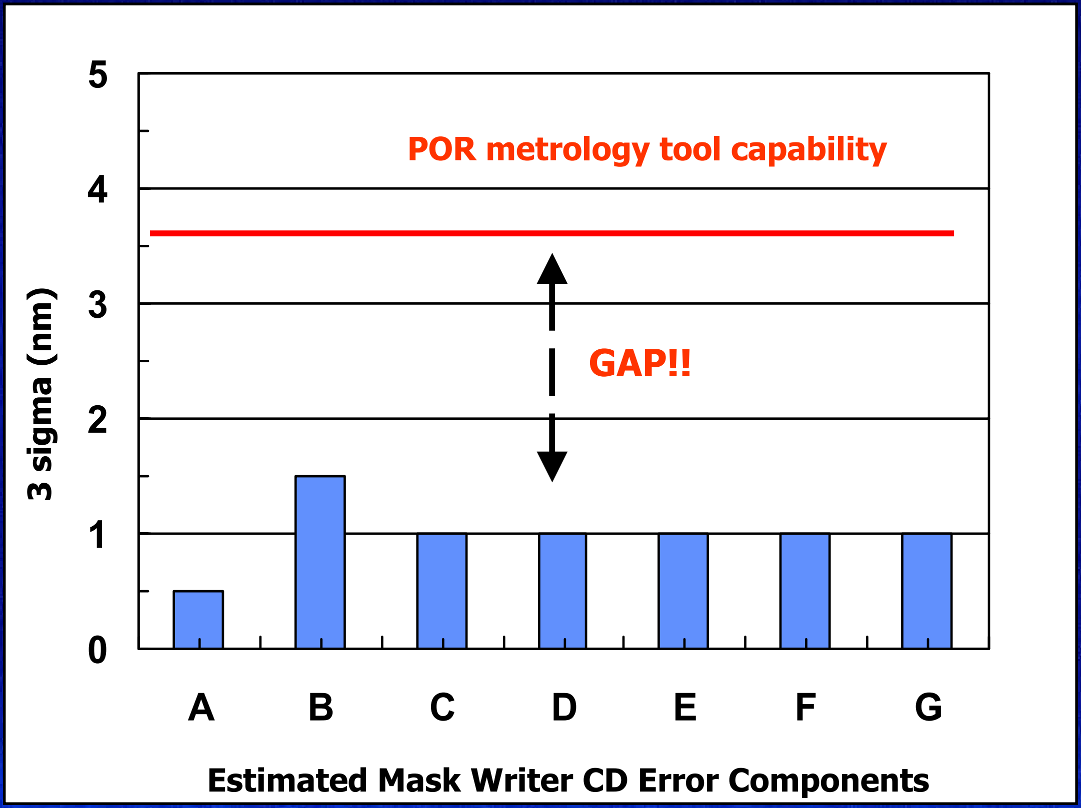
65nm Node Lithography

Mask Making Challenges – 193nm

Mask CD Control = Process CD Control



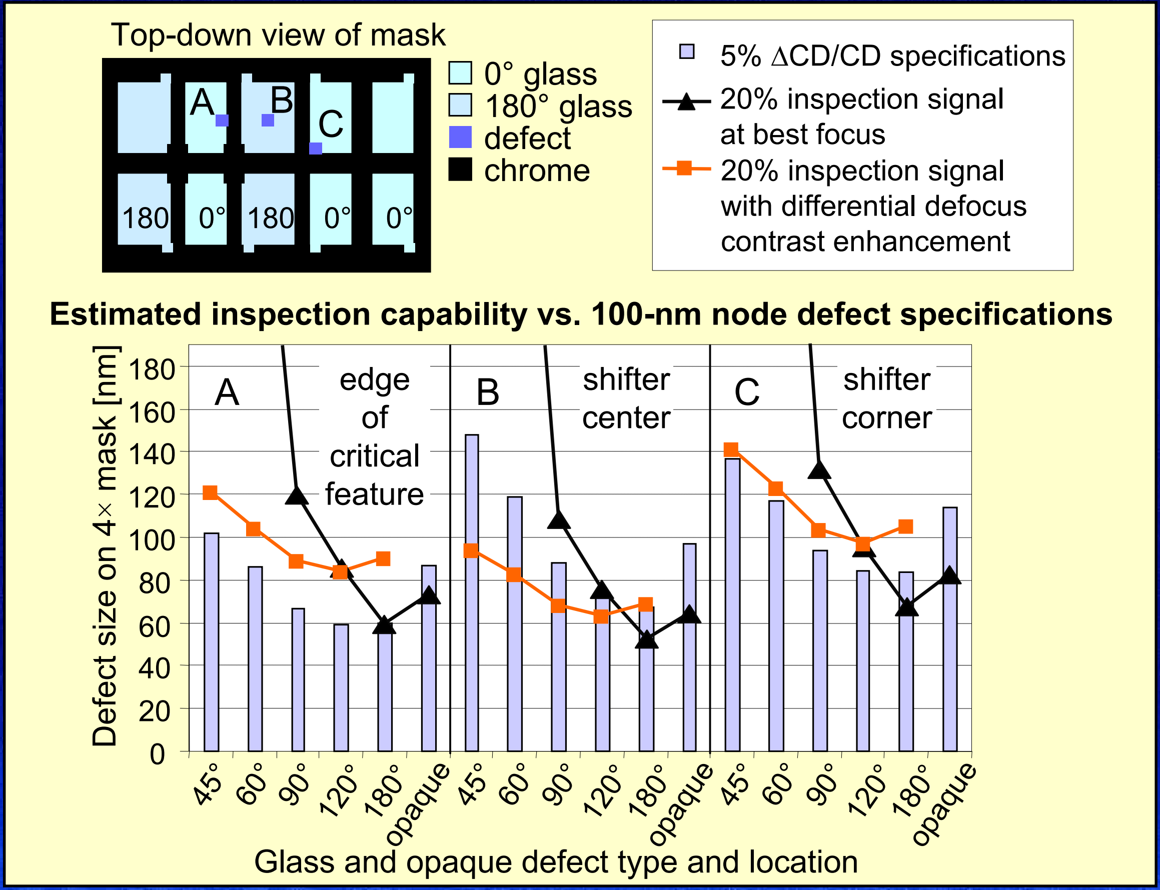
Lack of CD SEM Precision Limits Mask Making CD Control Improvements.

Novel Metrology might be required to Support 65nm Node Mask making needs

65nm Node Lithography

Mask Making Challenges – 193nm

AltPSM Mask Inspection = Availability + Cost



Modeled Inspection capabilities vs 90nm Node Gate Layer Specifications
257nm, NA=0.7; σ=0.5

Planned Capabilities are not sufficient even for 90nm Node.

Major effort required for 65nm Node

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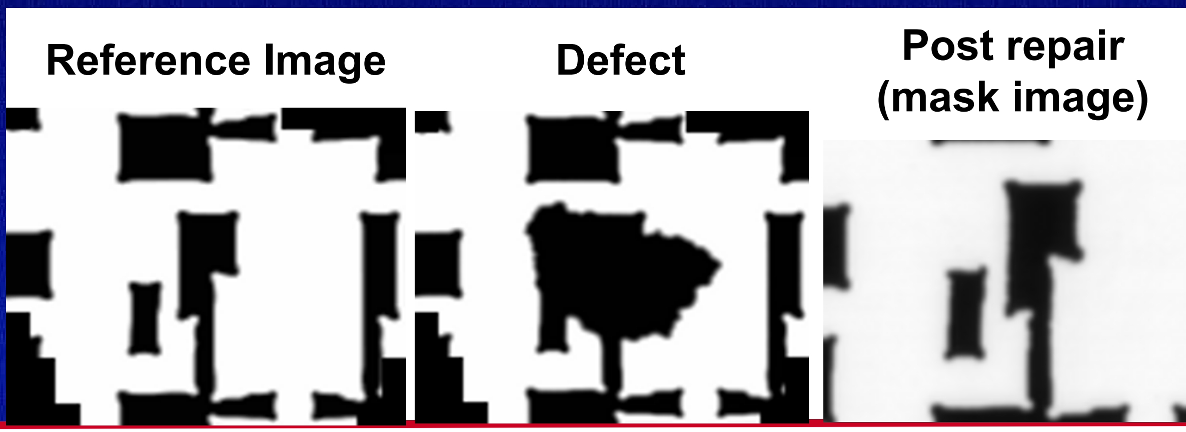
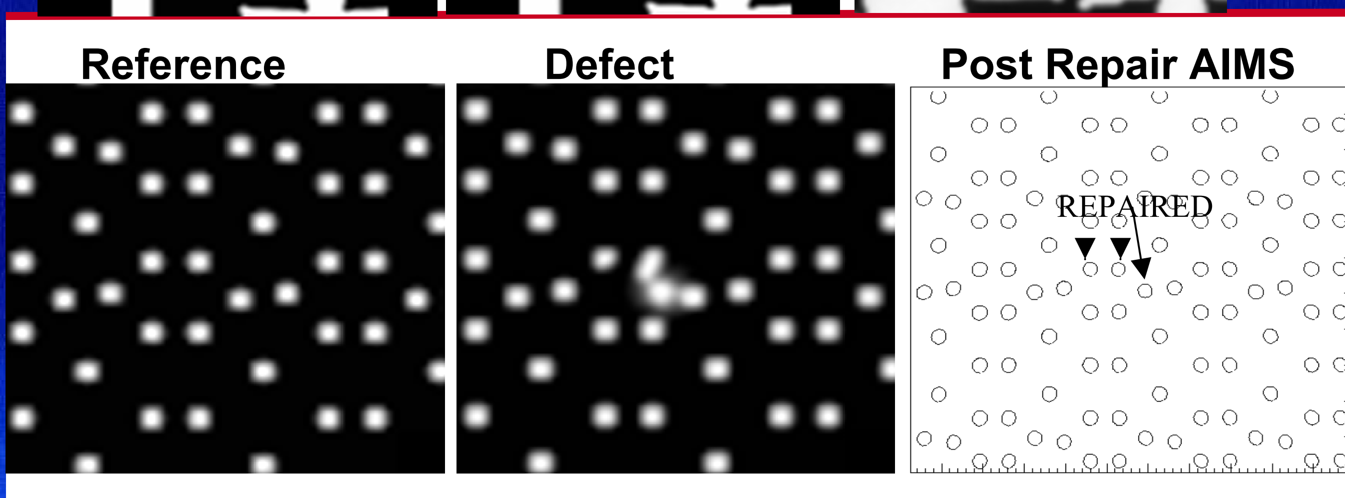
65nm Node Lithography
Mask Making Challenges – General

- **Repairs Capabilities = Availability + Cost**



Some 90nm Node Capabilities OK

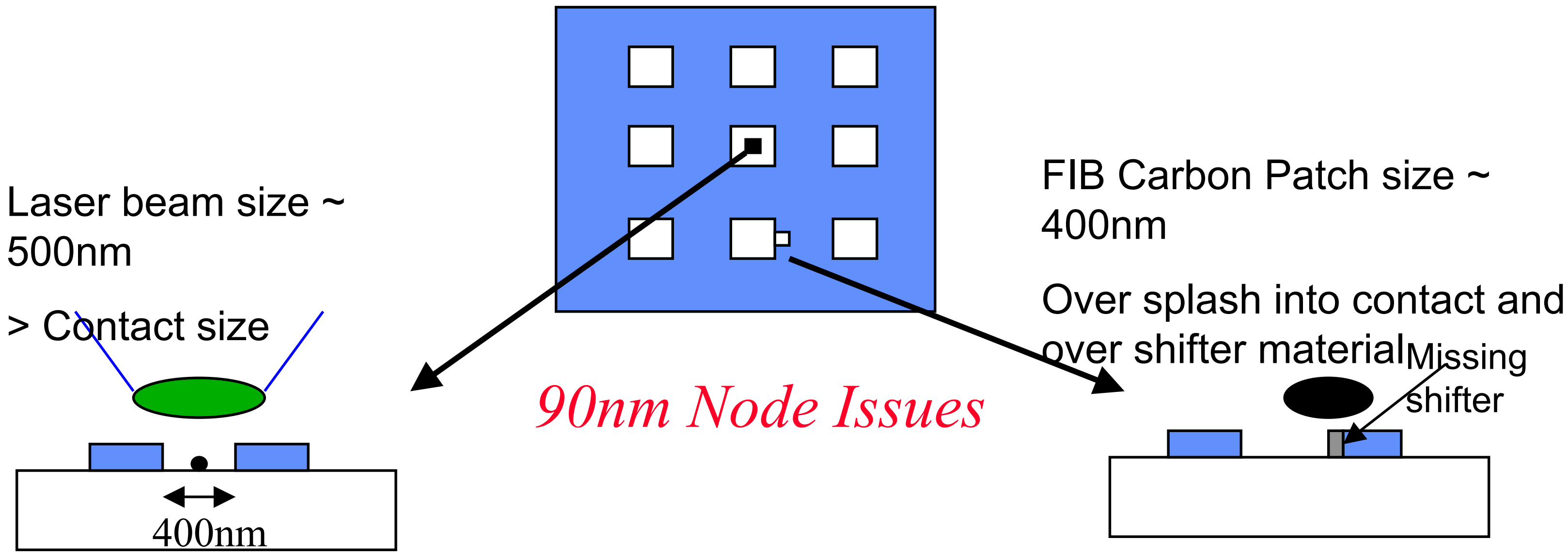
OPC Repair



EPSM Repair

65nm Node Lithography
Mask Making Challenges – General

- **Repairs Capabilities = Availability + Cost**



Limiter: Focus of small laser spot.

Poor image viewing resolution.

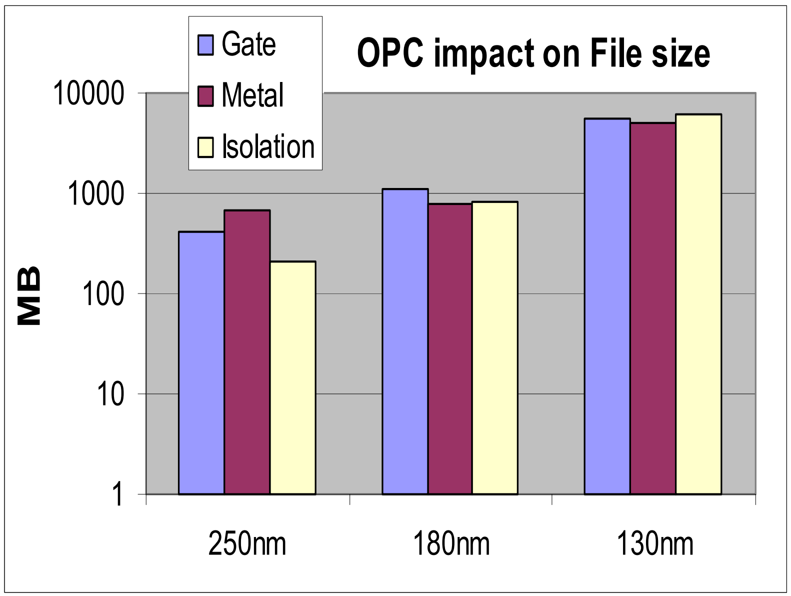
Cost effective laser repair solution not available even for 90nm node.

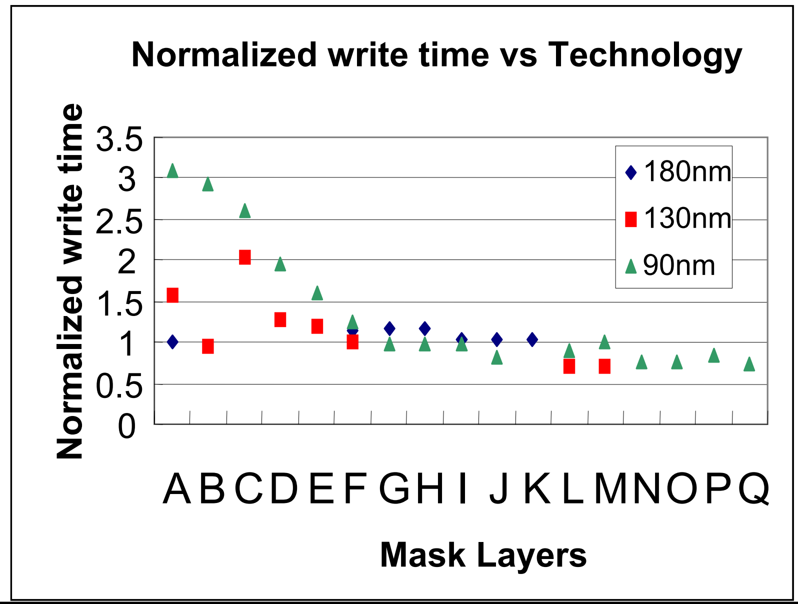
FIB tool barely meets 90nm timing.

65nm node tool needed : Q4/2002.

65nm Lithography
Mask Making Challenges – General

- **Data Structure = Availability + Cost**





Data Volume and Write time approach unaffordable levels.
New Hierarchical Data Stream formats suitable for distributed computing on scalable platforms are necessary for 65nm Node

Lithography Strategy for 65nm Node

Conclusions:

- 65 nm Lithography Node (160nm Pitch) requirements can be met by either 157nm or 193nm Lithography.
- 157nm Technology needs to stay on schedule and resolve particle protection issue to be inserted in 65nm Node Manufacturing with traditional patterning.
- 193nm Technology require wide use of "Strong" RET such as AltPSM to pattern tight pitches for 65nm Node. Significant advances in AltPSM mask making are necessary to support 65nm Node Manufacturing with AltPSM in 2005.
- Both 157 Particle protection issues and 193nm AltPSM mask making issues need to be resolved before 2005.

Lithography Strategy for 65nm Node

Acknowledgements

Asahi Glass Corporation, DuPont Co. and DuPont Photomask Inc for kind permission to use material from their respective presentations at 157nm technical data Review, Dec. 12-13, 2001, Orlando, FL, USA

Thank You !

Presentation and Manuscript pre-print posted on the Intel Silicon Showcase Website

Silicon Showcase
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http://www.intel.com/research/silicon/lithography.htm